Attorney Docket No. 1675B.1A.1

APPLICATION FOR U.S. PATENT TRANSMITTAL FORM

The Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventor(s) Ionel Jitaru

For: Low Noise Full Integrated Multlayers Magnetic For Power Converters

[X] Utility [ ] Design [ ] Plant

Enclosed are:

(1) 6 sheet(s) of formal drawings;
(2) Specification with claims;
(3) Application for U.S. Patent, Declaration, and Power of Attorney;
(4) A duplicate copy of this form;
(5) Check Number 3203 for the amount of $ 420.00 ;
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VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f)) - SMALL BUSINESS CONCERN

As the legal representative of Rompower Inc. a corporation under the laws of the State of Arizona, located at 4400 E. Broadway, ste. 414 Tucson, Arizona 85711, I hereby declare that it is a Small Business Concern, as defined in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code with regard to the invention entitled:Low Noise Full Intergrated Multlayer Magnetic For Power Converters,and filed Contemporaneously.

I further declare that exclusive rights to the invention have been conveyed to and remain with the above identified small business concern.

The Small Business above acknowledges its duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Signature: Ionel Jitaru Date: 11/05/1997

Name of Person Signing: Ionel Jitaru

Title: Low Noise Full Intergrated Multlayers Magnetic For Power Converters

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PATENT APPLICATION

LOW NOISE FULL INTEGRATED MULTLAYERS MAGNETIC FOR POWER CONVERTERS

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Docket No. 1675B.1A.1

"SPEC675B.1A1"

Nov. 4, 1999

LOW NOISE FULL INTEGRATED MULTILAYERS MAGNETIC FOR POWER CONVERTERS

BACKGROUND OF INVENTION

This is a continuation of United States Patent application serial number 08/351,943, filed on December 8, 1994, and entitled "Low Noise Full Integrated Multilayer Magnetic for Power Converters".

This invention relates to DC-to-DC converters, DC-to-AC, AC-to-AC and AC-to-DC converters. The major characteristic of this power conversion technique is that all the magnetic elements are implemented on the same multilayers structure, and the power transfer is made highly efficient and by minimizing the common mode noise..

There is a continuing industry demand for increasing power density, which means more power transferred in a given volume. A method for increasing the power transfer through the converter is to increase the switching frequency in order to minimize the size of magnetic and the capacitors. Using prior art topologies such as forward or flyback, which employ "hard" switching techniques, makes high frequency operation less efficient. The switching losses associated with switch elements, which turn on when there is a voltage across them, are proportional with the

switching frequency. An increase in switching frequency leads to an increase in switching losses and an increase in level of electromagnetic interference (EMI).

In order to overcome limitations in switching speeds, the prior art has devised a new family of resonant and quasi-resonant converters. In the case of quasi-resonant converters, the prior art technique consists of shaping the current or voltage to become half- sinusoidal and to perform the switching when the current or voltage reaches zero. The reactive elements, which contribute to shaping the current or voltage, are part of the basic circuit and are considered undesirable in classic topologies. An example of one such circuit can be found in Vinciarelli, "Forward Converter Switching at Zero Current", U.S. Patent 4,415,959. The technique utilized by Vinciarelli consists of adding a resonant capacitor across the fly wheeling diode to create a resonant circuit in combination with the leakage inductance of the transformer. During the ON time of the main switch, a current charges the resonant capacitor, When the current reaches zero, the main switch turns OFF in the primary of the transformer. The output inductor discharges the resonant capacitor, transferring the energy to the load. This topology exhibits several drawbacks which limit its utilization to power under 200W.

An other family of quasi-resonant converters which switch at zero voltage is described by F.C. Lee in high Frequency Power Conversion International Proceedings (April 1987), Intertec Communications, Ventura, California. These prior art circuits operate similarly to those described above with the exception that the main switch turns ON and OFF at zero voltage. This has the advantage across the main switch and the frequency modulation which is required for controlling the output power makes this topology unattractive.

New topologies structures which are refereed to as "Soft transitions Technologies" were

developed, in order to eliminate the limitations associated with Quasi-resonant and resonant converters, but still maintaining the advantage of soft commutations for the switching elements. Such technologies are described by Mr. Jitaru in "Fixed Frequency Single Ended Forward Converter Switching at Zero Voltage" U.S. Patent # 5,126,931 and in Square Wave Converter having an Improved Zero Voltage Switching Operation: U.S. Patent # 5,231,563. Using these topologies the converter operates at constant frequency, modulating the power by varying the duly cycle, the current and voltages on the switching elements are square-wave to decrease the current and voltages stress, the transitions are done at zero voltage conditions, and the power is transferred to the output, both during the ON time and OFF time.

These latest topologies have proven superior in respect of efficiency over the previous resonant and Quasi-resonant topologies have proven superior in respect of efficiency over the previous resonant topologies. However, the parasitic elements of the circuit such as leakage inductance and stray inductance, will negatively affect the efficiency due the circulating energy contained in these parasitic elements. Due to the inter winding capacitance of the transformer the common mode noise will be injected into the secondary. In planar, low profile magnetic required for low profile packaging the inter-winding capacitance is larger, and as result the common mode noise injected via these parasitic capacitance is larger.

Brief Summary of the Invention

The invention offers a construction technique of the main transformer which also extends to all the magnetic elements, wherein the parasitic elements of the circuit are minimized. In the same time the common mode current injected to the secondary via the inter winding capacitance is reduced and even eliminated . The construction technique claimed in this inventions offers a simple and low cost method in further suppressing the differential and common mode noise at the converter level. This novel construction technique offers an avenue in increasing the power density of the converter and allows full compliance with the safety agencies.

The planar multilayers magnetic is characterized by the use of flat copper spirals located on separate dielectric layers. Each layer can contain one turn or multiple spiral turns. The interconnection between the layers can be done by vias or an interconnecting heater. The insulator material can be laminated epoxy filled board, such as FR4 or different dialectic materials. The planar multilayers structure has been described by Mr. Alex Estrov in "Power Transformer Design for 1Mhz Resonant Converter" at High Frequency Power Conversion in 1986. However, by decreasing the height of the planar magnetic the footprint will increase inn order to maintain the same winding resistance . This will sacrifice the power density of the converter. In this invention the transformer winding is winding is buried between minimum two layers of dialectic and the space in top of the winding can be populated with surface mounted components for a better volumetric efficiency. The invention claims several winding structures in a planar transformer, designed to minimize the common mode noise. The inventions further claims a full integrated multilayers structure in which all the magnetic elements are located on the same multilayers structure. The winding arrangements in the input and output inductor are also

structured to minimize the common mode noise. It further utilizes the inter layers capacitance to create a low impedance for the common mode and differential mode noise, and to short it back to the source. To compensate for the common mode noise injected by the primary switching elements into the common baseplate to the secondary, the invention claims a noise cancellation technique by injected into the secondary a common mode current of the same amplitude but in opposite phase, through the common baseplate or through the multilayer structure. The invention claims a packaging configurations in which some the components of the converter are surface mounted, located on the same multilayers structure and for higher power applications cuts in the multilayers structure are performed to allow for the body of the power components. The heat-sink of the power components is connected to external heat-sinks.

Brief Description of the Drawings

Figure 1 is a cross-section view of the buried multilayers magnetic for a better volumetric efficiency.

Figure 2 is a top view if the assembled power converter using full integrated multilayers magnetic.

Figure 3B is an inner layer in the full integrated multilayers magnetic which contains a section of the input filter, winding, a section of the transformer's secondary winding and a section of the output inductor winding.

Figure 4 depicts the injection of the common mode current through the primary to secondary winding capacitance, due to the voltage gradient across the primary winding of the transformer.

Figure 5 presents the effect of a shield between primary and secondary winding in order to decrease the common mode current via the primary to secondary winding capacitance.

Figure 6 presents the use of a differential mode and common mode input choke together with two"Y" capacitors in order to reduce the common mode current flowing towards the input source.

Figure 7 presents a typical "sandwich" layer distribution in the transformer for a reduced leakage inductance and a reduced ac copper losses.

Figure 8 depicts a layer distribution aimed to decreased the common mode current injection to the secondary, by locating the secondary layers in between "quiet" primary layers. Quiet primary windings are those which exhibit a lower amplitude voltage swing in report to the primary ground.

Figure 9 presents a further common mode current reduction by using a shield between the secondary and two "quiet" primary layers.

Figure 10 presents a method for the cancellation of the common mode current into the secondary by locating the secondary layers between the "quiet " layer connected to the input DC voltage source and a "Noise cancellation winding" which creates a negative imagine of the common mode current injected by the first layer.

Figure 11 depicts a configuration in which the secondary windings are located between two symmetrical auxiliary windings, which are wound in a such way to cancel the common mode current injected to the secondary via the primary to secondary winding capacitance.

Figure 12 presents a configuration in which the switching element is connected in the middle of the primary winding, creating a perfect symmetry in which the common mode current injected into

the secondary winding via the primary to secondary capacitance is canceled.

Figure 13 depicts a winding arrangement in a magnetic element designed to reduce the inter-winding capacitance and for a better utilization of the copper. The width of each turns becomes larger as one moves form the inside turn to the outermost turn. In this way the winding resistance for the shorter turn can equal to the winding resistance for the longer turn. There is a shift between the layers to minimize the capacitance in between two adjacent layers.

Figure 14 presents a method of compliance with IEC950 in with three layers of core material are used, for example FR4, between the primary winding and secondary winding.

Figure 15 presents a second method of compliance with IEC950 wherein the core material in between primary and secondary winding has to be thicker than .4 mm.

Figure 16 depicts a method of compliance with safety agencies in which the magnetic core is reported to the primary and the transformer does not have to be buried. The secondary winding has to comply with the creapage distances in accordance with coating environment, based on the RMS voltages measured in the transformer.

Figure 17 presents a configuration in which multiple multilayers transformers on the same multilayers structure are utilized for higher power applications or for a reduced number of layers.

Detailed Description of the Preferred Embodiments

The multilayers planar magnetic, in which the windings are continuous flat copper spirals located on separate dielectric substrates, have been used before signal and data processing. In power conversion filed the multilayers magnetic started to be used since 1986. However, there are several limitation with multilayers magnetic which prevented this technology from a large utilization. Decreasing the height of the magnetic, by utilizing flat winding leads to an increased footprint. As a result a large portion of the board on which the multilayers planar magnetic is mounted, cannot be used for another purpose , having a negative impact on the volumetric efficiency. Another limitation associated with planar multilayers magnetic is the increased inter winding capacitance, which leads to higher switching losses on the switching elements and a larger common mode current injected to secondary via the capacitance between primary and secondary winding . The parasitic elements such as the leakage inductance can be decreased in planar multilayer technology, but there is still the negative effect of parasitic elements associated with the interconnection pins. The interconnection pins will add to the cost of the magnetic and also will contributed an increase in losses.

This now to Fig 1 wherein a methodology of the invention is illustrated . The planar windings of the magnetic 8 are incorporated in an multilayers PCB structure 16. The top and bottom layer of the multilayers board 16 are utilized for interconnection and for pads of power components 20, or for shielding purposes or different other interconnections. By burying the magnetic winding inside of multilayers construction the footprint of the magnetic is reduced to the footprint of the core. this will allow a better utilization of the board, increasing also the power density. By burying the magnetic inside of a epoxy filled multilayers structure such as multilayers PCB, the

creapage distances requirement in between the windings and the edge of the board or cuts will be decreased. This is due to the fact that the spacing between primary and secondary inside of multilayers PCB has to comply with the coating environment. These spacing are several times smaller than those in the air.

Another advantage of this construction technique is the fact that the inter connection between the magnetic elements, for example between the transformer and output choke are done through the same multilayers PCB, eliminating the need for inter connection pins. The power components can be located in top of the multilayers PCB, interconnecting with the magnetic winding through vias, or can be located on an external heatsink, using cuts in the PCB tailored to the body of power components as is depicted in Fig. 2. In Fig 2 is presented a full integrated multilayers PCB structure which incorporates all the magnetic elements such as the input filter 10, the main transformer 12, and the output choke 14. The body of the power components is accommodated by using cuts in the multilayers PCB structure. The connection of power components to the windings is done by through holes in which the terminals of the components can be soldered to. For lower power levels the power components are located in top of the PCB and through vias or large parallel pads a sow thermal impedance is created to the bottom of the multilayers PCB to which an external heatsink can be attached. The additional heatsink may not be required if there is an air flow in top of the converter.

The magnetic core 18, will have its legs penetrating through the multilayers PCB. The core will create a closed magnetic path with or without an air gap, function of the electrical topology which utilized.

In figure 3A is presented the structure of a inner layer which contains a section of the input choke

winding 22 and a section of the primary winding 24 of the transformer. The cores of the input choke 10, main transformer 12 and output choke 14, are penetrating through the multilayers PCB. The vias 26, are designed to interconnect the winding from different layers. Some of the vias are designed to interconnect the magnetic windings to the components located on top and bottom of the multilayers PCB.

In figure 3B is presented the structure of a inner layer which contains a section of the input choke winding 22, a section of the secondary winding of the transformer 28 and a section of the winding of the output choke 30. The connection from the transformer to output choke is done directly without supplementary interconnections, This will minimize the stray inductance associated with the interconnection pins.

One of the novelty claimed by this invention is the integration of all the magnetic elements on the same multilayers structure and for a better utilization of the space, the magnetic windings are buried inside, allowing the top and bottom layer to be utilized for locating surface mounted components. This leads to a very efficient utilization of the volume due to a three dimensional utilization . This form of integration leads to a minimization of the interconnection impedance and as result leads to a higher efficiency in power processing.

The multilayers PCB magnetic offers a good avenue in addressing the creapages and clearance requirements demanded by the safety agencies. By burring the transformer inside of PCB as is depicted in fig 14, the spacing between primary and secondary is determined in accordance with the RMS voltages in transformer applied to a coating environment. These spacing are several times smaller than those in the air . However, between primary and secondary windings two or three layers of core material 92, 94, 96 is demanded, each two able to withstand

the dielectric test. Another method requires the core material between the primary and secondary 98, to be at least .4mm. The magnetic core can be reported to the primary or to the secondary. In Fig 16 is presented a case in which the core is reported to the primary. The secondary winding 104 are buried inside and the distance from the secondary winding 104 to the edge of the core slot has to comply with the creapage requirements for the RMS voltage measured in the transformer. Using this method the primary winding 102 and the interconnecting vias do not have to be buried in the multilayers PCB.

The AC voltage gradient across each turn of the winding is equal, but reported to the input ground the amplitude of the voltage swing increases from the turn connected to the input DC source to the maximum level to the turn connected to the switching element. As is depicted in Fig. 4. the voltage swing 32 across the primary winding, injects a current in the secondary winding 38 via the primary to secondary winding capacitance 34, 36. This current is further flowing through the decoupling capacitor 40, through the earth ground 44, returning through the connections of the input and output leads of the power supply and is a noise parameter that is measured by the FCC and VDE.

One method in suppressing some of the common node noise is utilizing a shield 54, or two located in between primary and secondary winding and connected to the input DC source or the input ground. The method is depicted in Fig.5. The capacitance between the shield 54 and the primary winding creates a low impedance path for the common mode current created by the AC voltage across the primary winding 32. However the stray impedance of the shield itself will create a voltage gradient across it which will inject a common mode current via the capacitance 56 between the shield and the secondary winding 38. This common mode current 42, is reduced

in comparison to the structure without the shield. However, the parasitic inductance of the connection to the input DC source 46, is critical for shielding effectiveness. One of the major drawback associated with the use of the shield is the fact that an increased parasitic capacitance will be created across the primary winding and across the secondary winding. This will increase the switching losses on the switching elements. This parasitic capacitance 52 will be in parallel with the inter winding capacitance of the primary and the parasitic capacitance of the switch itself. The switching losses will become more significant at higher operation frequency and for high input voltage applications such as Off-line converters.

In Fig 7 is presented a winding arrangement in a converter in which the secondary windings 80 are sandwiched between the primary windings. For simplicity, I consider that the primary winding of the transformer is contained in four layers and the secondary winding in one layer. The winding of layer 1 connected to the input voltage source 72, exhibit a lower voltage swing reported to the input ground comparative to the winding 78 of layer 4 connected to the switching element 70. In this particular case the voltage swing reported to the primary ground is four times larger for layer 4, 78 than for the layer 1, 72. It is logical to locate the secondary 80 in the vicinity of the "quiet" primary such as 72. However the secondary has to be located symmetrically in between primary windings for two reasons. One reason is to minimize the magnetic field intensity in between winding for lower AC copper loss, and the second reason is to lower the leakage inductance between primary and secondary. In order to decrease the common mode current injection into the secondary via the capacitance between primary winding to secondary winding, and maintaining in the same time the sandwiched structure, the configuration of Fig 8 is suggested. In Fig 8 the secondary winding is located between two "Quiet" layers. The

voltage swing across layer 1 is much smaller than the voltage swing across layer 3. This structure does not eliminate the common mode injection to the secondary but it will reduce it. The advantage of this configuration is the fact that it does not require any addition layer. In Figure 9 is presented a configuration in which two layers in top and bottom of the secondary are used as a shield. The location of the shield in vicinity of two "quiet" layers 1, 72 and layer 2, 74 will not increase significantly the parasitic capacitance across the primary winding. However two layers of the multilayers structure will be allocated to the shield.

A configuration which can reduce the common mode noise injection to the secondary to zero is depicted in Fig 10. In this configuration a noise cancellation winding 82, is added. The polarity of the voltage swing across this winding is in opposite to the polarity of the voltage swing across the wining in a layer 1. As result the common mode current injected into the secondary winding will be canceled. This method will require only one additional layer and if a perfect geometrical symmetry can be accomplished, the common mode current injected in the secondary can be totally canceled. The single drawback of this is the fact that one layer will be allocated just for the noise cancellation.

In Figure 11 is presented a configuration in which two layers are added, one in top and one in the bottom of the secondary winding. This windings have a common symmetrical connection which is connected to the input ground. The connection can be also to the input DC voltage source. The voltage swing across the winding 1, 84 and auxiliary winding 2, 86 will inject a common mode current into the secondary, but of the opposite polarity of each other. As a result the total common mode current injected to the secondary will be zero. These auxiliary windings can be utilized to provide power in the primary section such as the necessary bias

power, or can provide the power for the primary reported output.

Another path for the common mode current is through the capacitance between the switching elements in the primary and in the secondary, and the baseplate. This applies for higher power applications in which a common heatsink baseplate is used for the power components in primary and secondary. Due to a large voltage swing of the power switch tab, this source of common mode noise can be dominant. This invention claims a method for cancellation of the common mode current produced by the switching elements. This is done by creating a supplementary capacitor between secondary and the termination of the noise cancellation winding not connected to the input DC source or input ground. The noise cancellation windings are described in Fig. 10 and Fig 11. By properly tailoring this additional capacitance a current will be injected into the secondary, of the same amplitude but in opposite phase to the current injected by the switching elements to the secondary via the capacitance between the switches and the baseplate. The additional capacitance between the noise cancellation winding and secondary can be implemented in the metal baseplate or in the multilayers structure.

Another method which does not require supplementary layers for output common mode noise cancellation is presented in figure 12. In this case the primary winding is symmetrically cut in a half and the power switch is connecting to these sections. The voltage swing on the layers which surrounds the secondary, layer 2, 74 and layer 3, 76, will have the same amplitude but will be of opposite polarity. As a result the common mode noise injected into the secondary will be zero.

The structures presented above will reduce the common mode noise injection to the secondary via the inter winding capacitance of the transformer. However, if the common mode

noise will be generated by different circuitry or if a further reduction of common mode is required, a supplementary common mode filter may be required. Such a structure is described in Fig 6. By utilizing a EE or EI core gapped in the center leg, the input choke can exhibit a common mode and a differential mode impedance. By using the outer legs of the Encore, two inductive elements can be implemented in the PCB. The coupling in between these inductor will determine the CM impedance, and it can be tailored by the gaping configuration of the core. For example, if there is not a gap in the core, the coupling coefficient is K =.071. If there is 1 mill gap in all the legs, K=.276. If only the center leg is gaped to 2 mil, K=.724. The common mode and differential mode inductance can be tailored by properly gapping the core, and making sure that under all loading conditions the core does not saturate, Utilizing full integrated multilayers PCB, the cost of the input EMI filter is reduced to the cost of the magnetic core. The capacitors 62, and 64 are used to create a low impedance for the common mode current which will work against the high impedance exhibited by the input filter. The capacitors 62 and 64 can be created in the structure of the multilayers PBC, which will lead to a cost reductio of the converter and to a better utilization of the multilayers structure. These capacitors can be constructed to comply with the safety agencies by using the recommendations suggested for the transformer compliance with safety agencies, previously discussed.

In figure 13 is presented a method for reduction of the parasitic capacitance across the magnetic winding. This is accomplished by shifting the adjacent layers. For a better utilization of the copper, the turn width will vary in such a way to ensure an equal resistance per each turn. The turn width is made larger as one moves from the inside turn to the outermost turn.

For higher power applications or in applications which require large currents multiple planar

multilayers transformer can be utilized on the same multilayers structure as in depicted in Fig 17. The number of layers in primary 112, 114, 116 and in the secondary 118, 120, 122 of these transformers 106, 120, 122 can be reduced to one, which will allow the use of two layer multilayers structure. Another advantage of this configuration is the fact that the leakage inductance in each transformer can be very low, which will make this configuration ideal for high current and low output voltage.

Many alternations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. therefore, the invention must be understood as being set forth above only for the purpose of example and not by way of limitation. The invention is defined by the following claims wherein means may be substituted therein for obtaining substantially the same result even when not obtained by performing substantially the same function in substantially the same way.

What is claimed is:

1. A power processing device comprising:

a) a multilayer printed circuit board having multiple layers of dielectric sheets;

b) a first transformer having,

1) a first core extending through said layers of dielectric sheets, and,

2) a first set of electrically conductive windings, at least one of said windings of said first set of electrically conductive windings contained between two adjoining layers of said dielectric sheets;

c) a second transformer having,

1) a second core extending through said layers of dielectric sheets, and,

2) a second set of electrically conductive windings, at least one of said windings of said second set of electrically conductive windings contained between two adjoining layers of said dielectric sheets; and,

d) at least one electrically conductive trace extending between said first set of electrically conductive windings and said second set of electrically conductive windings, said at least one electrically conductive trace totally contained between two adjoining layers of said dielectric sheets.

2. The power processing device according to claim 1, further including a first shielding layer disposed on a first exterior surface of said multilayer printed circuit board above said first set of windings.

3. The power processing device according to claim 2, further including a second shielding layer disposed on a second exterior surface of said multilayer printed circuit board below said first set of windings.

4. The power processing device according to claim 1, wherein said first set of electrically conductive windings and the second set of electrically conductive windings are electrically encapsulated.

5. The power processing device according to claim 4, wherein said at least one electrically conductive trace is electrically encapsulated.

6. The power processing device according to claim 1,

a) wherein said first set of electrically conductive windings include quiet windings; and,

b) wherein said first transformer further includes a secondary set of windings positioned to have electrical flow induced therein by said first core, said secondary set of windings positioned proximate to said quiet windings.

7. The power processing device according to claim 1,

a) wherein said first transformer further includes a secondary set of windings positioned to have electrical flow induced therein by said first core; and,

b) further including an open loop positioned to inject a current through parasitic capacitance in said secondary windings having a polarity opposite that of current in said first set

of windings.

8. The power processing device according to claim 1,

a) wherein said first transformer further includes a secondary set of windings positioned to have electrical flow induced therein by said first core; and,

b) further including an open loop positioned proximate and on a second side of said secondary windings.

9. The power processing device according to claim 1,

a) wherein said first transformer includes a secondary winding;

b) wherein said second transformer includes a secondary winding;

c) wherein the secondary winding of said first transformer and the secondary winding of said second transformer are electrically connected in parallel; and,

d) wherein the first set of electrically conductive windings and the second set of electrically conductive windings are electrically connected in series.

10. A power processing device comprising:

a) a multilayer printed circuit board having multiple layers of dielectric sheets;

b) a transformer having,

1) a core extending through said layers of dielectric sheets, and,

2) a first set of electrically conductive windings, at least one of said windings of said first set of electrically conductive windings contained between two adjoining layers of said dielectric sheets; and,

c) a first shielding layer disposed on a first exterior surface of said multilayer printed circuit board above said first set of windings.

11. The power processing device according to claim 10, further including a second shielding layer disposed on a second exterior surface of said multilayer printed circuit board below said first set of windings.

12. The power processing device according to claim 11, further including an electrically conductive trace contained between two layers of said dielectric sheets, said conductive trace communicating with said first set of electrically conductive windings.

13. The power processing device according to claim 10, further including:

a) a set of quiet windings contained within said first set of windings; and,

b) a secondary set of windings positioned to have electrical flow induced therein by said

core, said secondary set of windings positioned proximate to said quiet windings.

14. The power processing device according to claim 10, further including:

a) a secondary set of windings positioned to have electrical flow induced therein by said core; and,

b) an open loop positioned to inject a current through parasitic capacitance in said secondary windings, said injected current having a polarity opposite that of current in said first set of windings.

15. The power processing device according to claim 10, further including:

a) a secondary set of windings positioned to have electrical flow induced therein by said core; and,

b) further including an open loop positioned proximate and on a second side of said secondary windings.

Abstract:

A multilayer structure in which all the magnetic elements have the windings edged in the inner layers and the magnetic core which surrounds the winding has the legs penetrating through the multilayer structure. The interconnection between the magnetic elements and the rest of electronic components is done through the layers of the multilayer board, horizontally and vertically through via. For higher power components special cuts are performed in the multilayer board to accommodate the body of the components which may be connected to an external heatsink. The winding arrangement in the transformer is done in a such way to minimize and even eliminate the common mode noise injected through the capacitance between primary and secondary winding. The input filter is constructed to exhibit a differential and a common mode impedance. Supplementary capacitors are incorporated in the multilayers structure to offer a low impedance to the noise to short it to the source, or for injecting currents of opposite polarity to cancel the common mode current transferred through the transformer's inter winding capacitance and through the parasitic capacitance of the switching elements to the secondary. The insulation between winding can be in accordance with the safety agency requirements, allowing much shorter creapage distances inside of the multilayer PCB structure than in the air due to the compliance with coating environment.

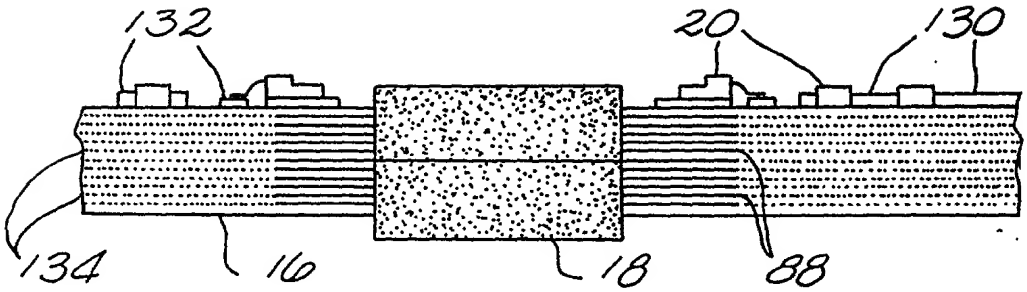

FIG. 1

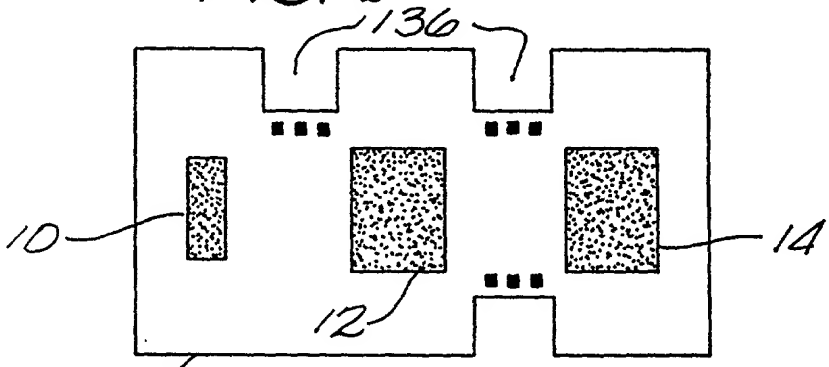

FIG. 2

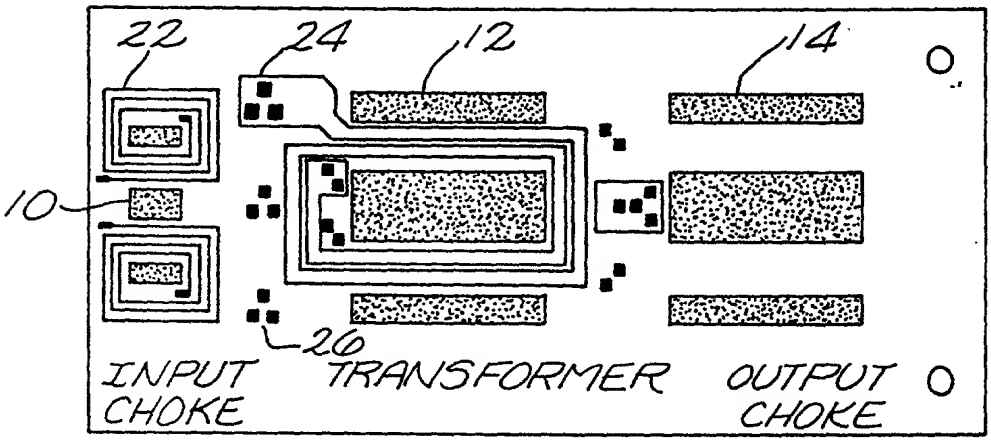

FIG. 3A

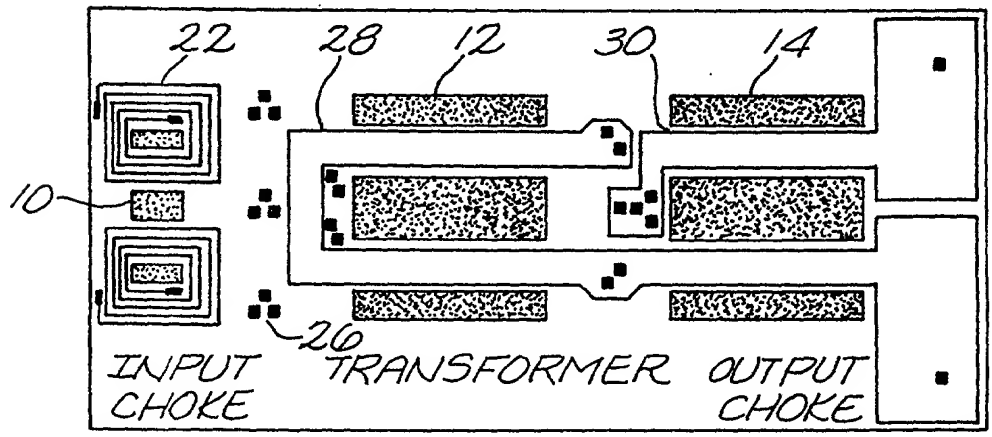

FIG. 3B

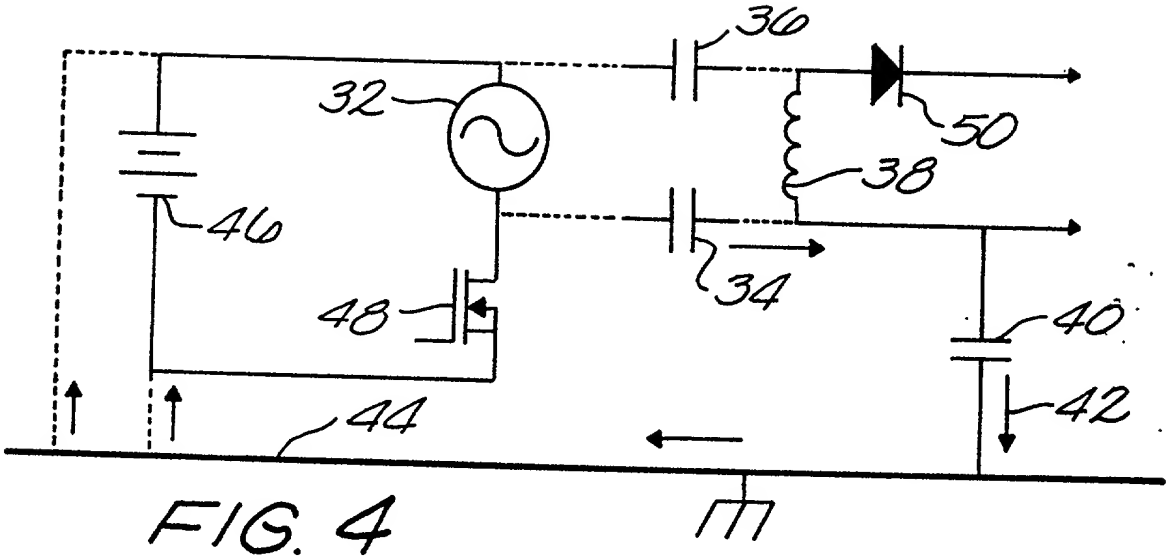

FIG. 4

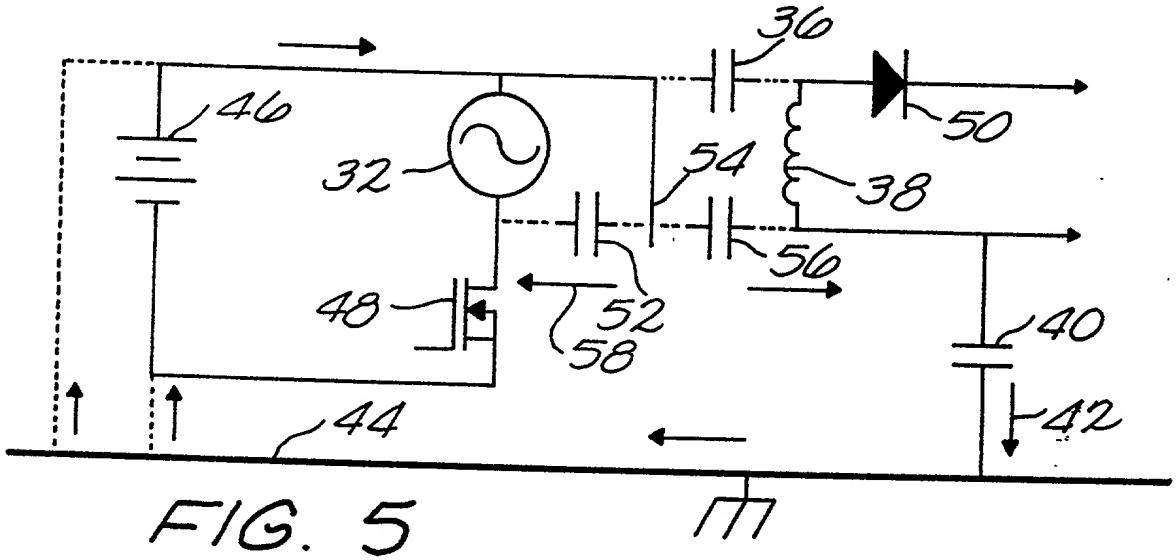

FIG. 5

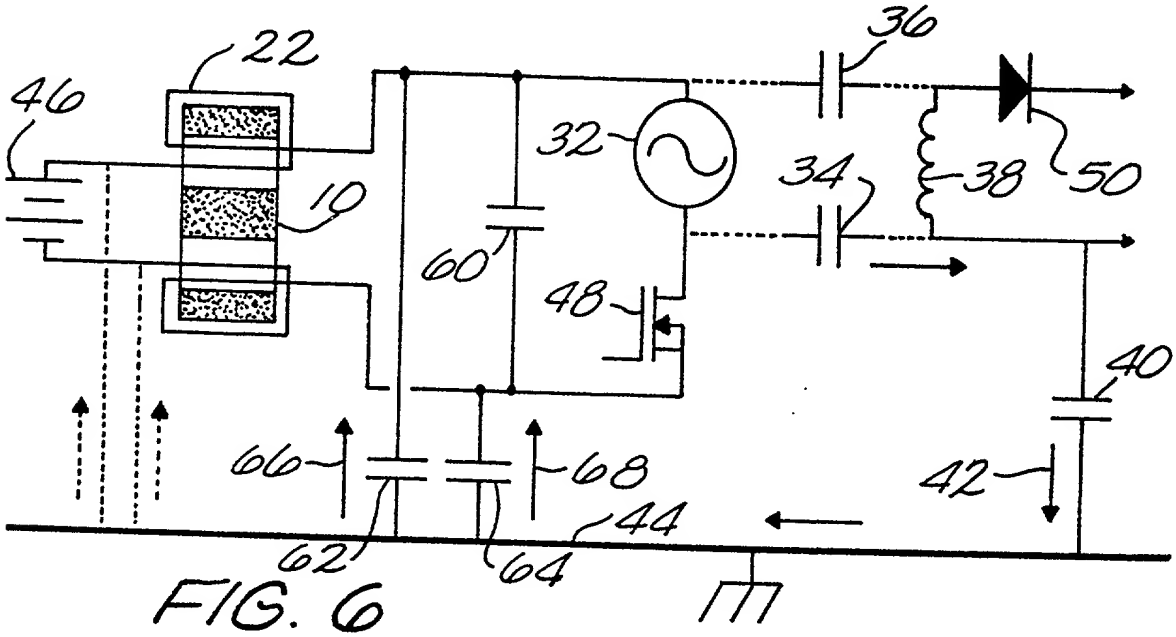

FIG. 6

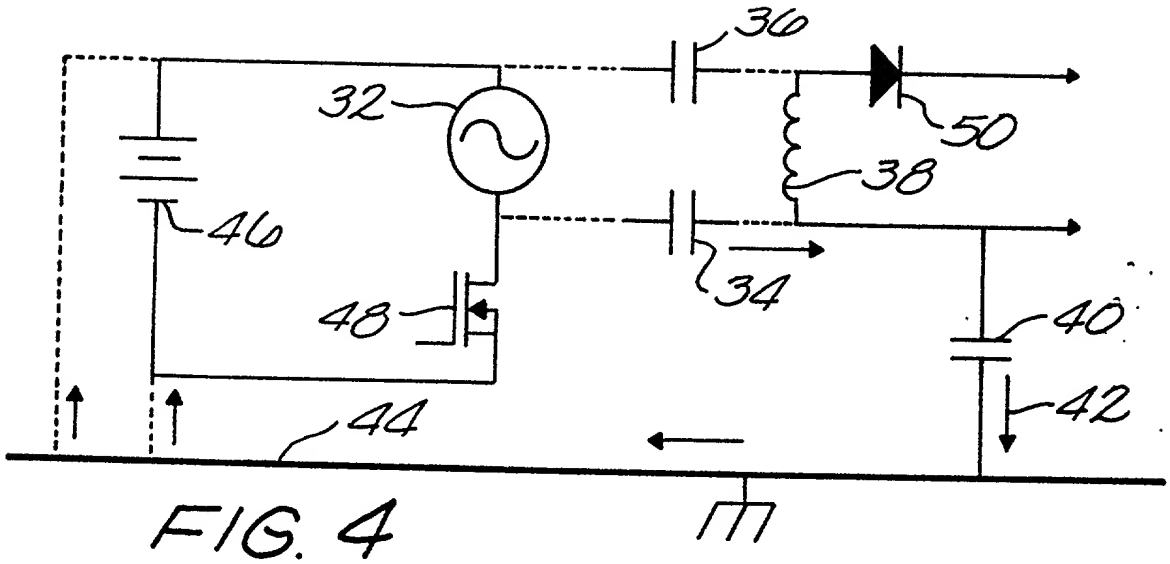

FIG. 4

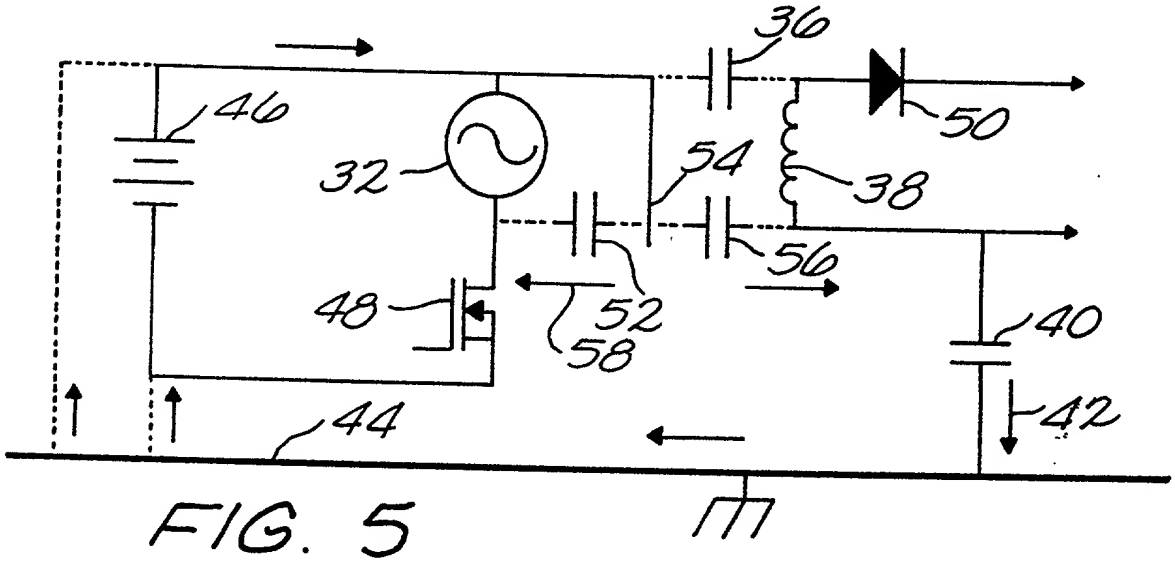

FIG. 5

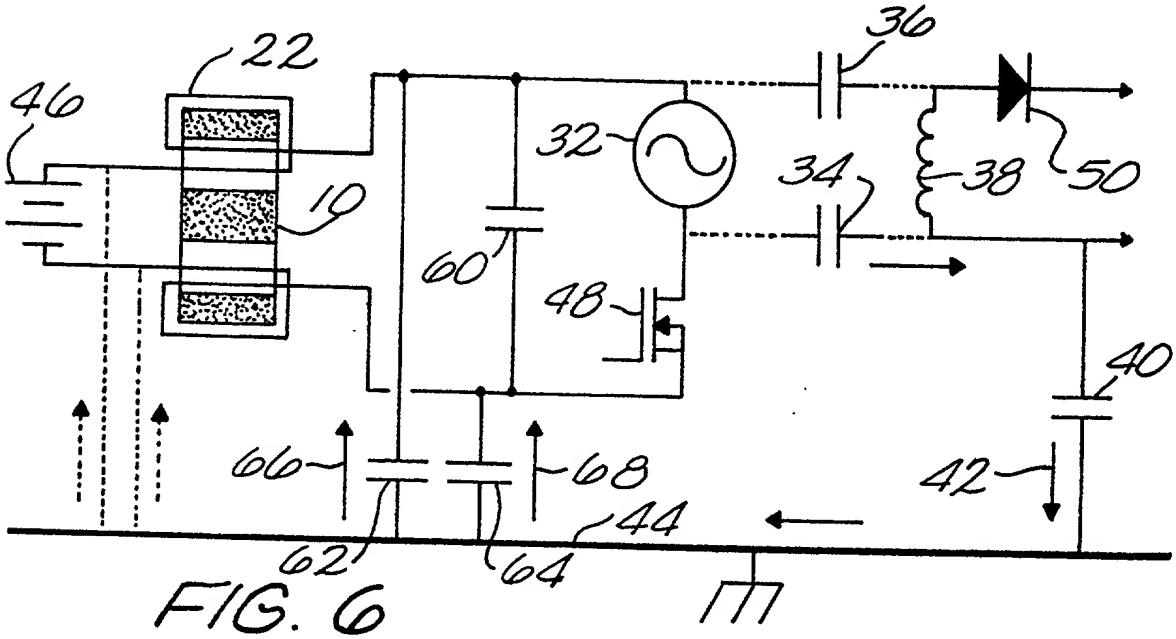

FIG. 6

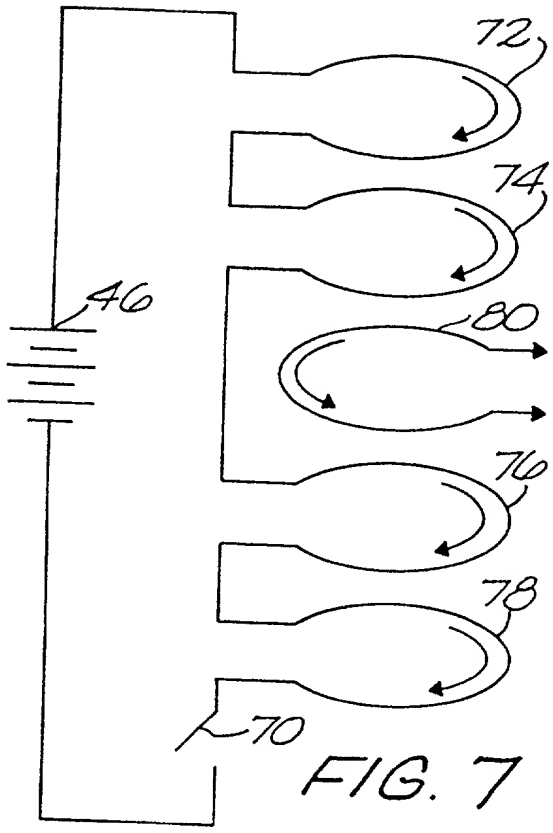

FIG. 7

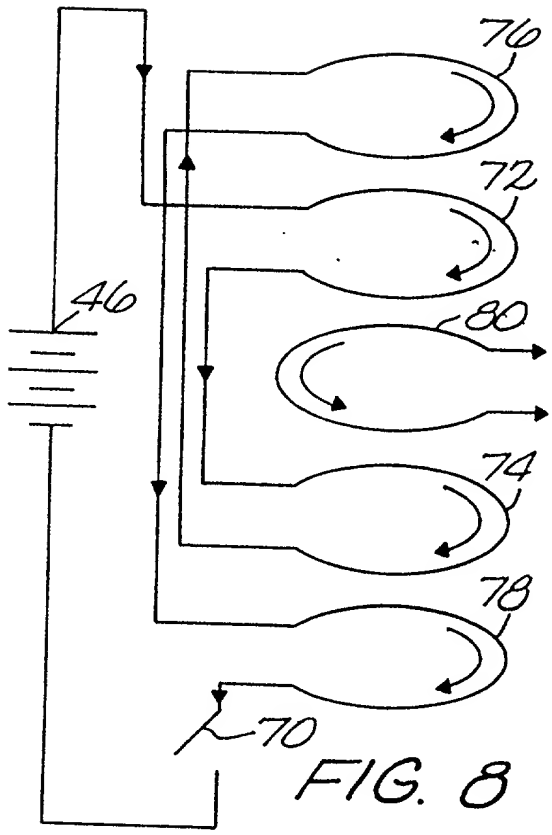

FIG. 8

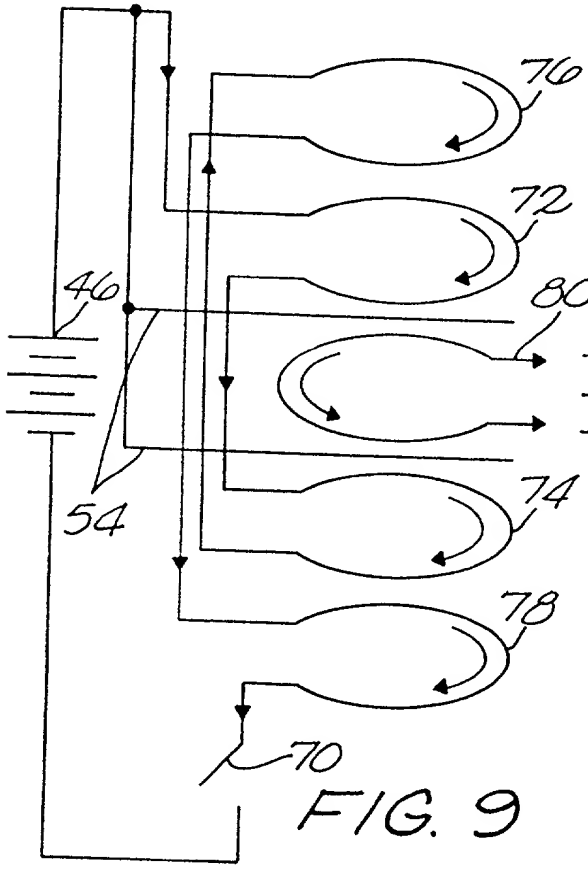

FIG. 9

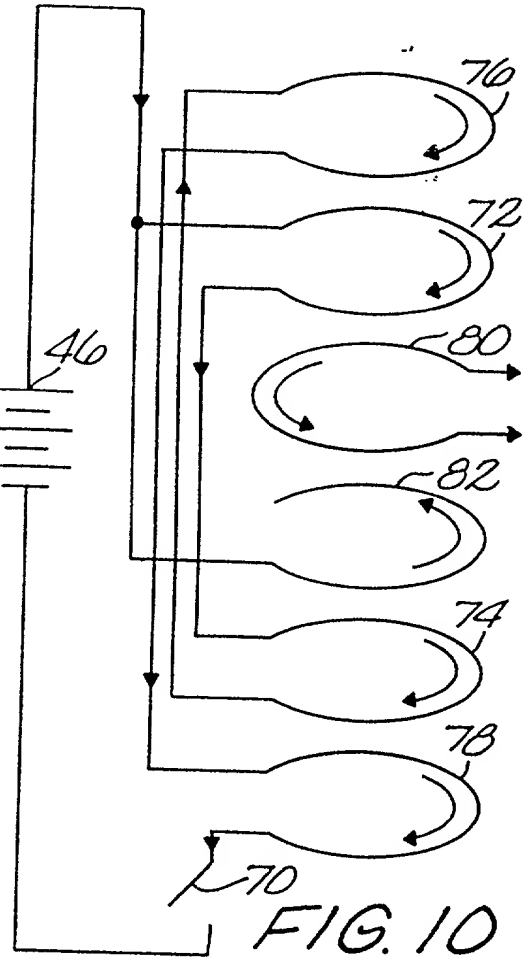

FIG. 10

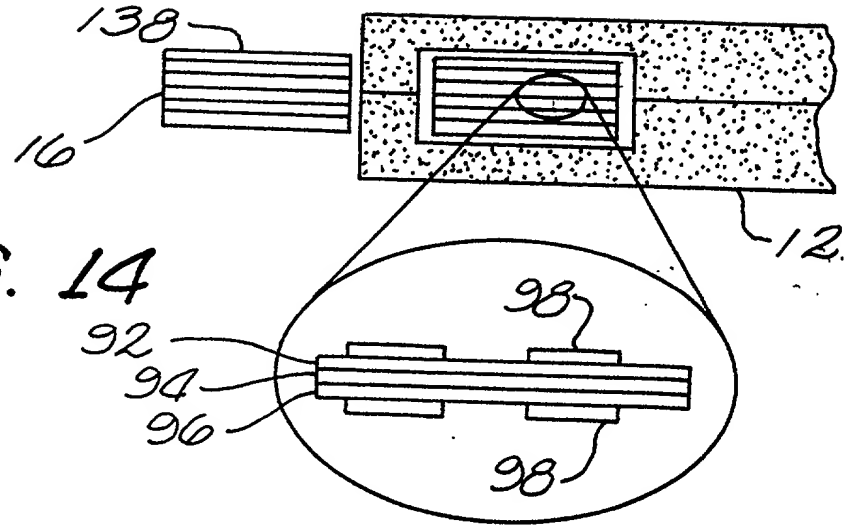

FIG. 14

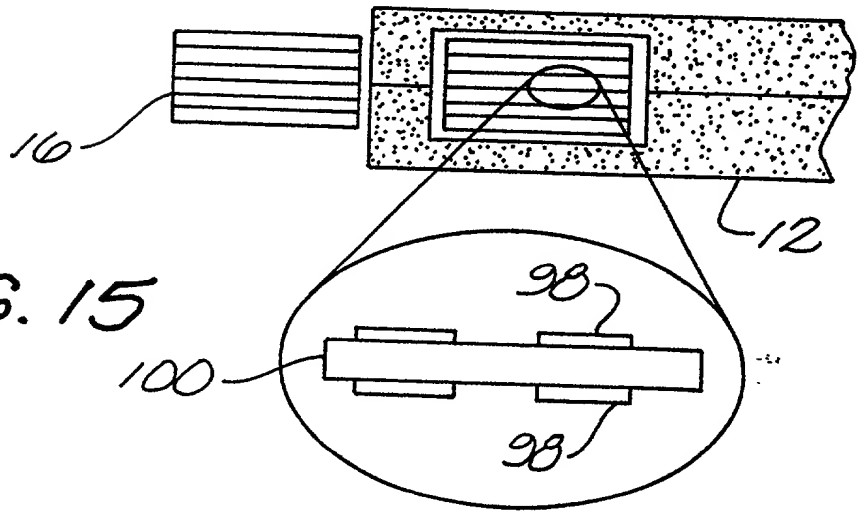

FIG. 15

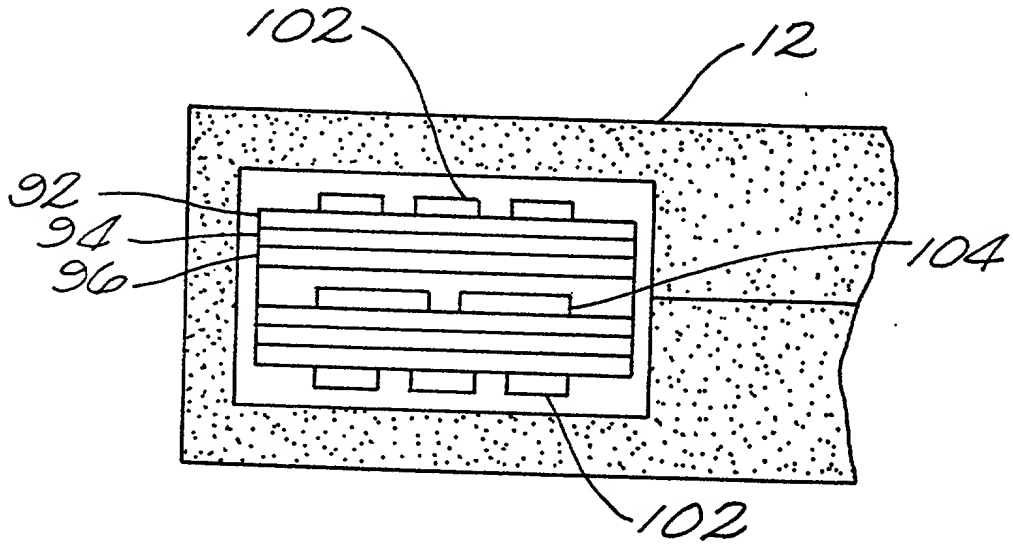

FIG. 16

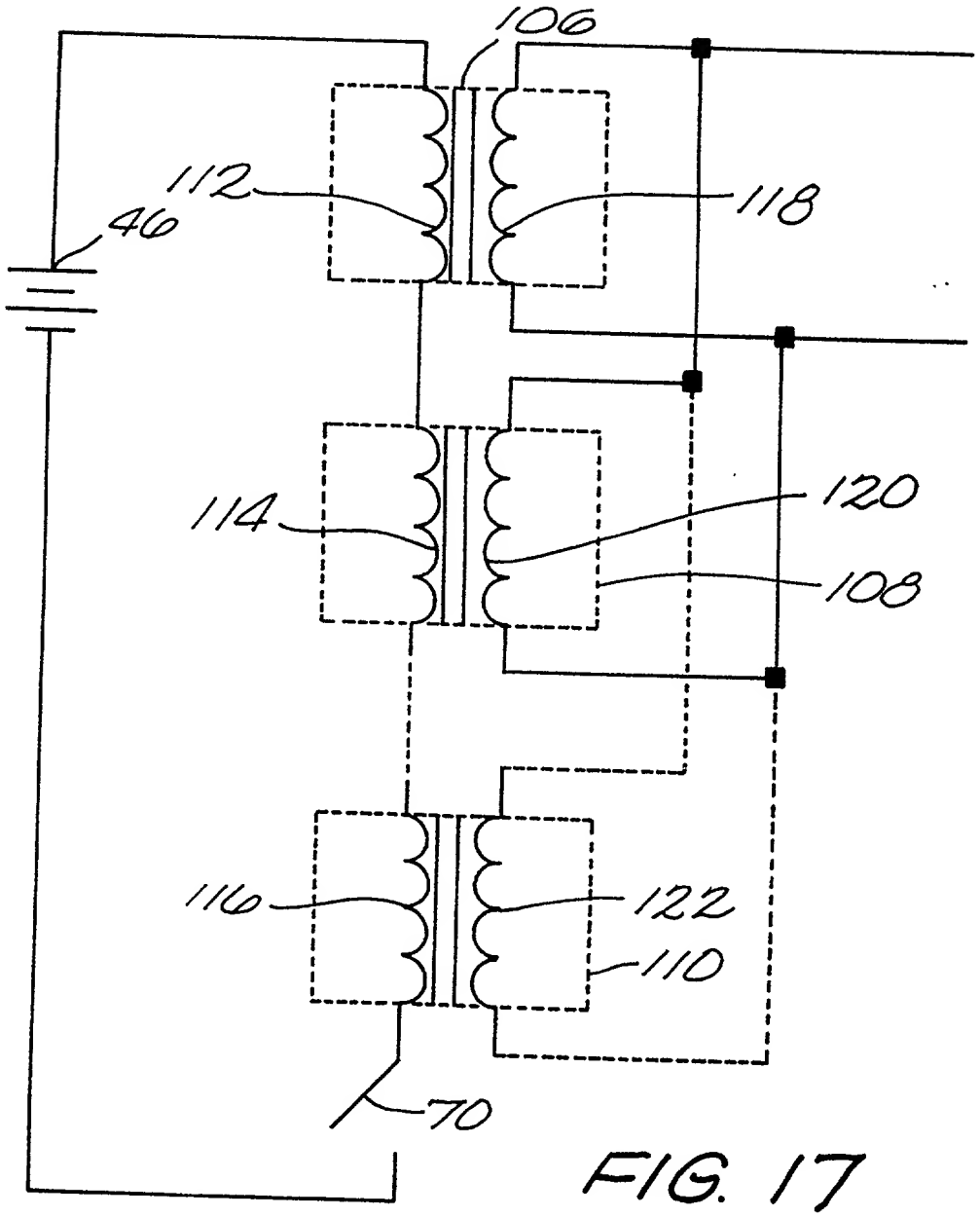

FIG. 17

1675B.1A.1
Attorney Docket No.

APPLICATION FOR U.S. PATENT
DECLARATION AND POWER OF ATTORNEY

As the below named inventor(s), I/we declare that my/our residence, post office address, and citizenship are as stated below next to my name; that I/we have read and understand the contents of the attached specification, including the claims as amended by any amendment specifically referred to herein; that I/we verily believe that I/we am/are the original, first and sole inventor(s) of the invention entitled as set forth below, which is described and claimed in the attached specification; that I/we do not know and do not believe that the same was ever known or used in the United States of America before my/our invention thereof, or patented or described in any printed prior publication in any country before my/our invention thereof, or more than one year prior to this application; or in public use or on sale in the United States of America more than one year before the date of this application; that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me/us or my/our legal representatives or assigns more than twelve months prior to this application; that no application for patent or inventor's certificate on the invention has been filed by me/us or my/our legal representative(s) or assigns in any country foreign to the United States of America; and that I/we acknowledge my duty under 37 CFR 1.56(a) to disclose information of which I/we am/are aware which is material to the examination of this application.

TITLE OF INVENTION: Low Noise Full Integrated Multlayers Magnetic For Power Converters

INVENTOR(S):

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Residence: 2378 N. Sun Lake Place (street) Tucson, (city) Arizona (state) 85769 (zip)

Post Office Address: SAME AS ABOVE

Citizenship: USA

POWER OF ATTORNEY: As the named inventor(s), I/we hereby appoint the following attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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Mark Ogram: (520) 574-3399

I/we further declare that all statements made herein of my/our own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor(s): Donald J. Haru

Date: 11/05/1999